

FIELD-PROVEN COTS, MOTS AND CUSTOM MILITARY POWER SOLUTIONS

M9526 SERIES 28V SWITCH MODULE



PRODUCT HIGHLIGHTS

- Short Circuit Current Limit Adjustable
- Overload Breaking Current Adjustable
- I2C Communication
- Discrete Operation
 Option







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Electrical Specifications

DC Output DC Input

Input: 0 to 50 V_{DC} • Input-to-Output impedance: Less than 2.5 mΩ @ 25 °C

Vcc: 3 to 5.5 Vpc • Max load capacitance per channel:

3 mF

Vcc Supply Current: 25mA Typical

Output

• Overload Breaking Current Adjustable from 2A to 30 A according to I2T curve.

• Short Circuit Current Limit Adjustable from 10 A to 125 A

according to SCL curve.

Control

• I2C Communication see • Open drain fault discrete signal

• On/Off discrete signal

EMC

Complies with MIL-STD-461F (50µH LISN): RE102, CE102, CS101¹, CE101¹, CS114¹,

CS115¹, CS116¹, RS103¹

Note 1: Tested with full system

Environmental 1

Design to Meet MIL-STD-810G

Temperature Operating: -55°C to +125°C at

ambient

Storage: -55°C to +125°C

Altitude

Method 500.5, Procedure I & II Storage/Air Transport: 40 kft

Operation/Air carriage: 70 kft

Fungus

Does not support fungus growth, in accordance with the guidelines of

MIL-STD-454, Requirement 4.

Humidity

Method 507.5, Up to 95% RH

Shock1

Salt Fog:

Method 509.5

Method 516.6

40g, 11msec saw-tooth (all

directions)

Vibration¹

Figure 514.6E-1. General minimum integrity exposure. (1 hour per axis.)

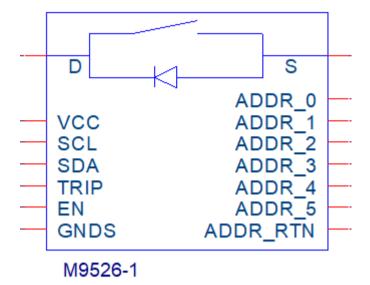
Note 1: Tested with full system

Reliability

2,529,861 hours, calculated IAW MIL-HDBK-217F Notice 2 at +85°C, Ground fixed conditions.

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Functions and Signals



| Signal No. | Signal Name | Description | | | |
|------------|-------------|--|--|--|--|
| 1 | VCC | Control supply voltage with respect to GNDS. | | | |
| 2 | SDA | I2C bus Data. | | | |
| 3 | SCL | I2C bus Clock. | | | |
| 4 | TRIP | Open drain fault discrete signal. See Figure 1. | | | |
| 5 | EN | The Enable signal is used to turn the SWITCH BRICK ON and OFF. | | | |
| 6 | ADDR_0 | Used for Slave Device Addressing | | | |
| 7 | ADDR_1 | Used for Slave Device Addressing | | | |
| 8 | ADDR_2 | Used for Slave Device Addressing. | | | |
| 9 | ADDR_3 | Used for Slave Device Addressing. | | | |
| 10 | ADDR_4 | Used for Slave Device Addressing | | | |

| 11 | ADDR_5 | Used for Slave Device Addressing. | | | |
|----|---|---|--|--|--|
| 12 | ADD_RTN | Used for Slave Device Addressing. | | | |
| 14 | GNDS | ground for I2C, TRIP, EN and VCC. | | | |
| 15 | D | Drain for Power Path. For positive voltage switch it will be the input voltage side connection. | | | |
| 16 | Source for Power Path. For positive voltage switch it will be the I connection. | | | | |

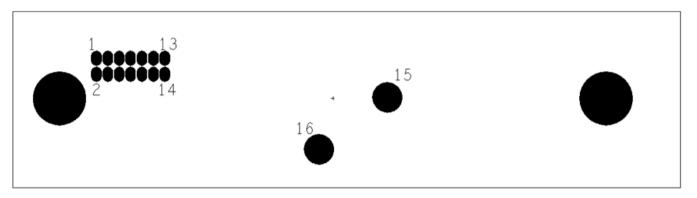
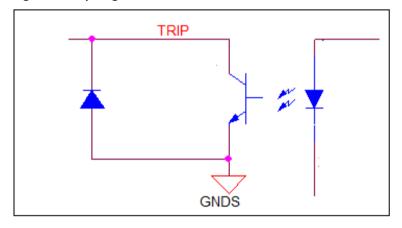


Figure 1 – Trip stage



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1. Typical Tests Results

2. Typical Characteristics

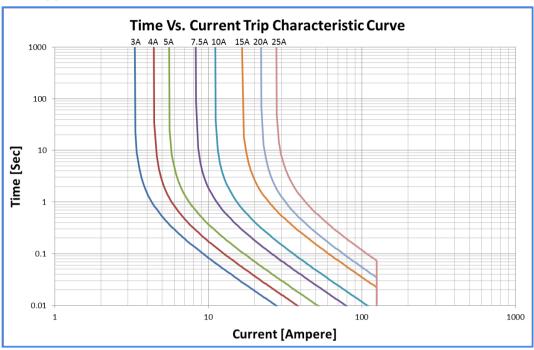


Figure 2 - Time vs. Current Trip

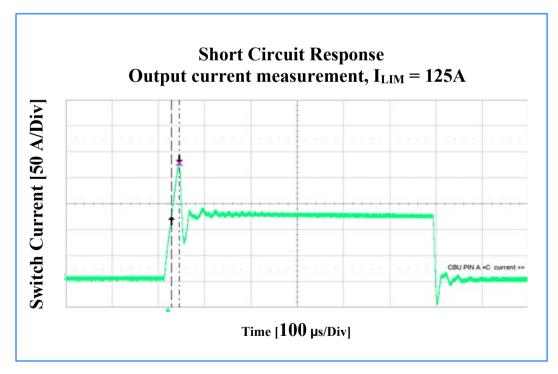


Figure 3 - Short Circuit Response

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1. I2C Protocol

Slave Address:

For $0 \le ADDR \le 7 \rightarrow ADDR + 0x70$

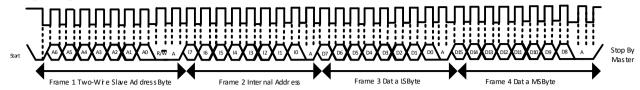
For other Address = ADDR

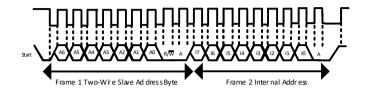
Slave will be read as a memory device with one byte of internal address.

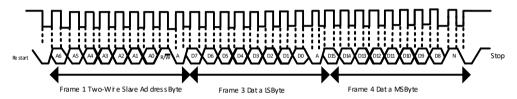
Byte order shall be little endian. For example, 01h address will be the LSB of VOUT1.

| Internal Address | Name | Function | R/W | Number of bytes | notes |
|---------------------|---------|-------------------------------------|-----|-----------------|---|
| 00h | STAT | Status Register | R | 1 | STAT[0] = Reset Flag (RST) STAT[1] = Switch State ('1' = ON) STAT[2] = Trip Status ('1' = Fault) STAT[3] = Short Status ('1' = Trip from short circuit) STAT[4:7] = Reserved |
| 01h | OUTCURR | Load Current Measurement | R | 2 | LSB = 62.5mA |
| 03h | VOLTD | Voltage Drop Measurement | R | 2 | LSB = 62.5mV |
| 05h | TEMP | Temperature Measurement | R | 2 | LSB = 0.0625°C |
| 07h | 12TACC | I ² t Status | R | 3 | I ² t accumulator with respect to I2T_LIM |
| Oah | CTRL | Control Register | RW | 1 | CTRL[0] = Switch Enable ('1' = En) CTRL[1] = Trip Reset ('1' = Reset) CTRL[2] = Reset Flag (RST, Reset value = '1') CTRL[4:7] = Battle Mode (0xD = Battle Enable) |
| 0bh | OLCL | Overload Current Limit | RW | 2 | LSB = 62.5mA |
| Odh | I2T_LIM | Maximal I ² t Setting | WR | 3 | Thermal Constant(TC) is the trip time for twice of the overload current setting. I2TACC can be set by following formula: I2TACC = (IOVERLOAD*16) ² *TC*16 TC [s], IOVERLOAD [A] |
| 10h | SCCL | Short Circuit Current Limit | RW | 2 | LSB = 62.5mA |

Timing Diagram

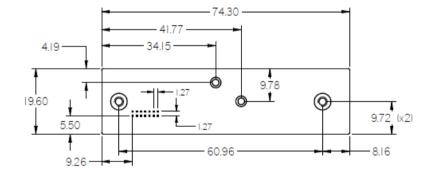


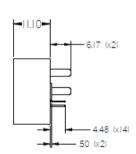




A[0:6] – Address D[0:15] – Data I[0:7] – Internal Address A – ACK N – NACK

Outline Drawing





Notes

1. Dimensions are in mm

2. Weight: 32g

3. 3D model available

Standard Configurations

| | Input | Output | | |
|-------------|-------------------------|--------------------------|--------------------|------------|
| Part Number | Input Voltage range | V _{cc} | Voltage | Current |
| M9526-100 | 0 to 50 V _{DC} | 3 to 5.5 V _{DC} | Following Input | Adjustable |

Note: Specifications are subject to change without prior notice by the manufacturer.

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